BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	3	"2209857"	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 10:12
2	BRS	L2	3	(data with (transfer$4 or exchang$4) with core with share$2).clm.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 10:25
3	BRS	L3	5	(cad or cam or computer adj2 aided adj2 design or tool) same librar$2 same (interconnect$4.3 or connect$4 or exchang$4 or transfer$4) same shared adj5 (memory or memories or RAM)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 10:31
4	BRS	L4	1	(cad or cam or computer adj2 aided adj2 design or tool) same librar$2 same (interconnect$4.3 or connect$4 or exchang$4 or transfer$4) same shared adj5 (memory or memories or RAM) same logic	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 10:32

	Type	L #	Hits	Search Text	DBs	Time Stamp
5	BRS	L5	1	((cad or cam or computer adj2 aided adj2 design or tool) and librar$2 and (interconnect$4.3 or connect$4 or exchang$4 or transfer$4) and shared adj5 (memory or memories or RAM) and logic).ab.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 10:32
6	BRS	L6	1	((cad or cam or computer adj2 aided adj2 design or tool) and librar$2 and (interconnect$4.3 or connect$4 or exchang$4 or transfer$4) and shared adj5 (memory or memories or RAM) and logic).clm.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 10:33
7	BRS	L7	21	((cad or cam or computer adj2 aided adj2 design or tool) and librar$2 and (interconnect$4.3 or connect$4 or exchang$4 or transfer$4) and (memory or memories or RAM) and logic).clm.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 10:33

	Type	L #	Hits	Search Text	DBs	Time Stamp
8	BRS	L8	18	((cad or cam or computer adj2 aided adj2 design or tool) and librar$2 and (interconnect$4.3 or connect$4 or exchang$4 or transfer$4) and (memory or memories or RAM) and logic and circuit$3).clm.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 11:17
9	BRS	L9	776	709/213.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 11:17
10	BRS	L10	76	9 and ((cad or computer adj2 aided adj2 design or tool) and (interconnect$4.3 or connect$4 or exchang$4 or transfer$4) and (memory or memories or RAM) and logic or circuit$3).clm.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 11:20

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L11	1	9 and ((cad or computer adj2 aided adj2 design or tool) and (interconnect$4.3 or connect$4 or exchang$4 or transfer$4) and (memory or memories or RAM) and (logic or circuit$3)).clm.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 11:20

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	46	709/213.ccls. and ((cad or computer adj2 aided adj2 design or tool) and (interconnect$4.3 or connect$4 or exchang$4 or transfer$4) and (memory or memories or RAM) and logic or circuit$3).ab.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 14:39
2	BRS	L2	1	709/213.ccls. and ((cad or computer adj2 aided adj2 design or tool) and (interconnect$4.3 or connect$4 or exchang$4 or transfer$4) and (memory or memories or RAM) and (logic or circuit$3)).clm.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 14:40
3	BRS	L3	1	709/213.ccls. and ((cad or computer adj2 aided adj2 design or tool) and (interconnect$4.3 or connect$4 or exchang$4 or transfer$4) and (memory or memories or RAM) and (logic or circuit$3)).ab.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 14:40

	Type	L #	Hits	Search Text	DBs	Time Stamp
4	BRS	L4	44	709/213.ccls. and ((cad or computer adj2 aided adj2 design or tool) and (interconnect$4.3 or connect$4 or exchang$4 or transfer$4) and (memory or memories or RAM) and (logic or circuit$3)).detd.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 14:41
5	BRS	L5	1	709/213.ccls. and ((cad or computer adj2 aided adj2 design or tool) same (interconnect$4.3 or connect$4 or exchang$4 or transfer$4) same (memory or memories or RAM) same (logic or circuit$3)).detd.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/20 14:41

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	0	system adj3 on adj3 chip	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/25 17:44
2	BRS	L2	15760564	system on a chip	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/25 17:45
3	BRS	L3	0	system adj5 on adj5 chip	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/07/25 17:45

Access DB# 127603

68

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name: __Jack Lane____ Examiner # :_68699__ Date: _07/20/04_____
Art Unit: _2188 Phone Number 305-3818___ Serial Number: 09/919,806_____
Mail Box Location: _2Y13___ Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: _Automatic generation of interconnect logic components

Inventors (please provide full names): see Bib sheet for inventor names_____

Earliest Priority Filing Date: 02/28/2001_____

***For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.**

See abstract and claims.

Search:
CAD (computer aided design) or tool
Circuit
Design or generation ?
Library?
Interconnect$ or connect# or exchange$
Shared and/or memory

****

STAFF USE ONLY

Searcher: Holloway
Searcher Phone #: 308-7794
Searcher Location: CPK2 4B30
Date Searcher Picked Up: 7-21-04
7-22-04

Type of Search

NA Sequence (#)_____
AA Sequence (#)_____
Structure (#) _____
Bibliographic ___v___
v

Vendors and cost where applicable

STN _____
Dialog ___v___
Questel/Orbit _____
Dr.Link _____
WWW v

```
Set     Items   Description
S1      20147   CAD OR CAE OR COMPUTER()AIDED()(TOOL? OR ENGINEER?) OR DES-
             IGN? OR ARCHITECTUR? OR SIMULAT? OR MODEL?
S2        167   VLSI OR FPGA? OR ISOC OR ISOCS OR SOC OR SOCS OR (LAB OR S-
             YSTEM OR COMPUTER)()"ON"(W1)(CHIP OR CHIPS) OR VHSIC OR LOGIC-
             ()DEVICE? OR GATE()ARRAY? OR LARGE()SCALE()INTEGRAT?
S3         81   (SHARE? OR DISTRIBUT? OR COMBIN?)(N)(MEMOR? OR STORAGE? OR
             SRAM OR ROM OR PROM OR EPROM)
S4      10932   INTERCONNECT? OR PIP OR PIPS OR CONNECT? OR EXCHANG? OR CO-
             RE? OR TRANSFER()PATH? OR CONNECT? OR BUS OR BUSES
S5      14565   LIBRAR? OR GROUP? OR STORED OR SAVE? OR REUS? OR RECYCL?
S6          0   (ARBITRAT? OR LEVEL? OR HIERARCH? OR LAYER?)(3N)S3
S7        129   S1 AND S2
S8          0   S7 AND S3
S9         48   S7 AND S4
S10        25   S7 AND S5
S11         0   S2 AND S6
S12         5   S1(3N)S2(4N)(S4 OR S5)
S13         0   S1 AND S6
S14        10   S7 AND S4 AND S5
S15        13   S12 OR S14
S16         3   S15 NOT PY>2001
S17         3   S16 NOT PD>20010228
File 256:SoftBase:Reviews,Companies&Prods. 82-2004/Jun
         (c)2004 Info.Sources Inc
```

17/3,K/1
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
(c)2004 Info.Sources Inc. All rts. reserv.

02705632 DOCUMENT TYPE: Company

ParthusCeva Inc (705632)
2033 Gateway Pl #150
San Jose, CA 95110-1002 United States
TELEPHONE: (408) 514-2900
FAX: (408) 514-2995
HOMEPAGE: http://www.parthusceva.com
EMAIL: info@parthusceva.com

RECORD TYPE: Directory

CONTACT: Sales Department

ORGANIZATION TYPE: Corporation
EQUITY TYPE: Public
STATUS: Active

SALES: NA

PERSONNEL: Fielding, Kevin, Chief Executive Officer; Fielding, Kevin, President; Wertheizer, Gideon, VP; Wertheizer, Gideon, Chief Technology Officer; Coughlan, Elaine, Chief Financial Officer; Ohana, Issachar, VP Sales
REVISION DATE: 20030330

ParthusCeva Incorporated's headquarters is in San Jose, California. Parthus **designs** and develops integrated circuit **design** software for mobile Internet devices, DSPs, and systems on chips (**SoCs**). Its IP **cores** underlie many of the electronics and semiconductor products of its business partners. Parthus's customers...

...The company was created from the former Parthus Technologies and the Ceva Division of DSP **Group** (Nasdaq: DSPG). It is a public company (NASDAQ: PCVA).

17/3,K/2
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
(c)2004 Info.Sources Inc. All rts. reserv.

01129259 DOCUMENT TYPE: Product

PRODUCT NAME: SOPC Builder (129259)

Altera Corp (512141)
101 Innovation Dr
San Jose, CA 95134 United States
TELEPHONE: (408) 894-7000

RECORD TYPE: Directory

CONTACT: Sales Department

REVISION DATE: 20031216

Altera's SOPC Builder streamlines the development of system-on-a-programmable-chip (SOPC) **designs** , automating system definition and integration processes. Employing SOPC Builder, users can define complete hardware and...

...systems quickly. The product also integrates with Altera (R) Quartus (R) II software, allowing programmable **logic** **device** developers to use the tool. SOPC Builder is included with the Nios (R) Development Kit and

Excalibur (TM) Solutions Pack products. The solution's **library** includes memory interfaces, **buses** , digital signal processing (DSP) **cores** , and other intellectual property (IP) and peripherals. SOPC Builder features processors as well as generic...

DESCRIPTORS: **CAD** ; **CAD CAM** ; **CAE** ; Circuit **Design** ; Computer Equipment ; DSP (Digital Signal Processors); Electrical Engineering; Electronics; PLCs; **SoC** (Systems on Chips)

```
Set     Items   Description
S1   14054940   CAD OR CAE OR COMPUTER()AIDED()(TOOL? OR ENGINEER?) OR DES-
             IGN? OR ARCHITECTUR? OR SIMULAT? OR MODEL?
S2     404777   VLSI OR FPGA? OR ISOC OR ISOCS OR SOC OR SOCS OR (LAB OR S-
             YSTEM OR COMPUTER)()"ON"(W1)(CHIP OR CHIPS) OR VHSIC OR LOGIC-
             ()DEVICE? OR GATE()ARRAY? OR LARGE()SCALE()INTEGRAT?
S3      44086   (SHARE? OR DISTRIBUT? OR COMBIN?)(N)(MEMOR? OR STORAGE? OR
             SRAM OR ROM OR PROM OR EPROM)
S4   18265786   INTERCONNECT? OR PIP OR PIPS OR CONNECT? OR EXCHANG? OR CO-
             RE? OR TRANSFER()PATH? OR CONNECT? OR BUS OR BUSES
S5   15311095   LIBRAR? OR GROUP? OR STORED OR SAVE? OR REUS? OR RECYCL?
S6         414   (ARBITRAT? OR LEVEL? OR HIERARCH? OR LAYER?)(3N)S3
S7         192   S1(S)S2(S)S3(S)S4
S8           0   S7(S)S6
S9          30   S7(S)S5
S10          0   S1(S)S2(S)S6
S11        187   S1(S)S6
S12        139   S1(5N)S2(5N)S3
S13          5   S11(S)S4(S)S5
S14         73   S12(S)(S4 OR S5)
S15         25   S12(5N)(S4 OR S5)
S16         60   S9 OR S13 OR S15
S17         33   RD (unique items)
S18         24   S17 NOT PY>2001
S19         24   S18 NOT PD>20010228
File 275:Gale Group Computer DB(TM) 1983-2004/Jul 22
         (c) 2004 The Gale Group
File  47:Gale Group Magazine DB(TM) 1959-2004/Jul 22
         (c) 2004 The Gale group
File 636:Gale Group Newsletter DB(TM) 1987-2004/Jul 22
         (c) 2004 The Gale Group
File  16:Gale Group PROMT(R) 1990-2004/Jul 22
         (c) 2004 The Gale Group
File 624:McGraw-Hill Publications 1985-2004/Jul 20
         (c) 2004 McGraw-Hill Co. Inc
File 484:Periodical Abs Plustext 1986-2004/Jul W1
         (c) 2004 ProQuest
File 613:PR Newswire 1999-2004/Jul 22
         (c) 2004 PR Newswire Association Inc
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 141:Readers Guide 1983-2004/Jun
         (c) 2004 The HW Wilson Co
File 239:Mathsci 1940-2004/Sep
         (c) 2004 American Mathematical Society
File 621:Gale Group New Prod.Annou.(R) 1985-2004/Jul 22
         (c) 2004 The Gale Group
File 674:Computer News Fulltext 1989-2004/Jun W4
         (c) 2004 IDG Communications
File  88:Gale Group Business A.R.T.S. 1976-2004/Jul 21
         (c) 2004 The Gale Group
File 369:New Scientist 1994-2004/Jul W2
         (c) 2004 Reed Business Information Ltd.
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 635:Business Dateline(R) 1985-2004/Jul 21
         (c) 2004 ProQuest Info&Learning
File  15:ABI/Inform(R) 1971-2004/Jul 21
         (c) 2004 ProQuest Info&Learning
File   9:Business & Industry(R) Jul/1994-2004/Jul 21
         (c) 2004  The Gale Group
File  13:BAMP 2004/Jul W2
         (c) 2004  The Gale Group
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 610:Business Wire 1999-2004/Jul 22
         (c) 2004 Business Wire.
File 647:CMP  Computer Fulltext 1988-2004/Jul W2
```

19/3,K/4 **(Item 4 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)

02268995 SUPPLIER NUMBER: 53871624 (USE FORMAT 7 OR 9 FOR FULL TEXT)
ARM Supports CoreFrame Architecture For SOC Designs. (Advanced RISC Machines supports PALMCHIP's processor architecture for system-on-chip design) (Company Business and Marketing)
Electronic News (1991), 45, 2256, 52(1)
Feb 8, 1999
ISSN: 1061-9577 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 309 LINE COUNT: 00029

ARM said the CoreFrame Architecture provides a proven system-on-chip **connection** methodology for data intensive **designs** , and adds to the range of **system - on - chip** technology supporting the ARM **architecture** .

CoreFrame uses a **shared memory architecture** which is optimized for devices with high bandwidth data streams requiring extensive direct memory access...

19/3,K/20 (Item 3 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01215650 CMP ACCESSION NUMBER: EET20000515S0094

Configurability is key to IP integration

Cary Ussery, Chief Executive Officer, Founder, Improv Systems, Beverly, Mass.

ELECTRONIC ENGINEERING TIMES, 2000, n 1113, PG126
PUBLICATION DATE: 000515
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: System Design - Focus: SOC: Design Tools
WORD COUNT: 1548

... signal-processing applications and advanced control processing.

The Jazz processor offers an innovative approach to **SoC design** -in particular to **design reuse** . The **architecture** was **designed** specifically for data- and computation-intensive applications such as video, audio and image processing and embedded **connectivity** . They typically require a high-performance data path and a state machine to control it...

...that this would be implemented best in a deep- submicron IC using a VLIW processor **architecture** and configurable logic and, since a central memory structure has no advantages, interspersed with **shared memories** . This cascade memory **architecture** allows compute resources to consume and produce data without bandwidth limitation, making possible simultaneous access...

```
Set      Items   Description
S1    13911102   CAD OR CAE OR COMPUTER()AIDED()(TOOL? OR ENGINEER?) OR DES-
             IGN? OR ARCHITECTUR? OR SIMULAT? OR MODEL?
S2      262166   VLSI OR FPGA? OR ISOC OR ISOCS OR SOC OR SOCS OR (LAB OR S-
             YSTEM OR COMPUTER)()"ON"(W1)(CHIP OR CHIPS) OR VHSIC OR LOGIC-
             ()DEVICE? OR GATE()ARRAY? OR LARGE()SCALE()INTEGRAT?
S3       44041   (SHARE? OR DISTRIBUT? OR COMBIN?)(N)(MEMOR? OR STORAGE? OR
             SRAM OR ROM OR PROM OR EPROM)
S4     3358464   INTERCONNECT? OR PIP OR PIPS OR CONNECT? OR EXCHANG? OR CO-
             RE? OR TRANSFER()PATH? OR CONNECT? OR BUS OR BUSES
S5     5005978   LIBRAR? OR GROUP? OR STORED OR SAVE? OR REUS? OR RECYCL?
S6         884   (ARBITRAT? OR LEVEL? OR HIERARCH? OR LAYER?)(3N)S3
S7        1744   S1 AND S2 AND S3
S8           0   S7 AND S4 AND S5 AND S6
S9          32   S7 AND S6
S10         30   S1(5N)S2 AND S3 AND S4 AND S5
S11         62   S9 OR S10
S12         47   RD (unique items)
S13         45   S12 NOT PY>2001
S14         45   S13 NOT PD>20010228
File   8:Ei Compendex(R) 1970-2004/Jul W2
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File 202:Info. Sci. & Tech. Abs. 1966-2004/Jul 12
         (c) 2004 EBSCO Publishing
File  65:Inside Conferences 1993-2004/Jul W3
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/Jul W2
         (c) 2004 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2004/Jun W4
         (c)2004 Japan Science and Tech Corp(JST)
File 111:TGG Natl.Newspaper Index(SM) 1979-2004/Jul 21
         (c) 2004 The Gale Group
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File   6:NTIS 1964-2004/Jul W3
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2004/Jul W2
         (c) 2004 INIST/CNRS
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Jul W3
         (c) 2004 Inst for Sci Info
File  62:SPIN(R) 1975-2004/May W4
         (c) 2004 American Institute of Physics
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Jun
         (c) 2004 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2004/Jun W1
         (c) 2004 FIZ TECHNIK
```

14/5/4 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04216498 E.I. No: EIP95072797996
Title: Parallel gate- level **circuit** simulation **on** shared memory architectures
Author: Bagrodia, Rajive; Chen, Yu-an; Jha, Vikas; Sonpar, Nicki
Corporate Source: Univ of California at Los Angeles, Los Angeles, CA, USA
Conference Title: Proceedings of the 9th Workshop on Parallel and Distributed Simulation (PADS'95)
Conference Location: Lake Placid, NY, USA Conference Date: 19950614-19950616
Sponsor: IEEE; ACM
E.I. Conference No.: 43319
Source: Parallel and Distributed Simulation, Workshop Proceedings 1995. IEEE, Los Alamitos, CA, USA,95TB8096. p 170-174
Publication Year: 1995
CODEN: 002093
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical); X; (Experimental)
Journal Announcement: 9509W4
Abstract: This paper presents the results of an experimental study to evaluate the effectiveness of parallel **simulation** in reducing the execution time of gate-level **models** of **VLSI** circuits. Specific contributions of this paper include (i) the **design** of a gate-level parallel **simulator** that can be executed, without any changes on both **distributed memory** and **shared memory** parallel **architectures** , (ii) demonstrated speedups with both conservative and optimistic **simulation** protocols (almost all previous studies on circuit **simulation** have failed to extract speedups with conservative protocols); in particular we showed that a speedup of about 3 was obtained on 8 processors of a Sparc1000 for conservative algorithms and about 2 for optimistic algorithms for circuits in the ISCAS85 benchmark suite; and (iii) performance comparison between **shared memory** and **distributed memory** implementations of the **simulator** . (Author abstract) 14 Refs.
Descriptors: Computer **simulation** ; Integrated circuit layout; **VLSI** circuits; Parallel processing systems; Computer **architecture** ; Computer hardware; Data storage equipment; **Simulators** ; Algorithms; Synchronization
Identifiers: Parallel gate **level** circuit **simulation** ; **Shared memory architectures**
Classification Codes:
723.5 (Computer Applications); 714.2 (Semiconductor Devices & Integrated Circuits); 722.4 (Digital Computers & Systems); 722.1 (Data Storage, Equipment & Techniques)
723 (Computer Software); 714 (Electronic Components); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

14/5/6 **(Item 6 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)

03703645 E.I. No: EIP93081064374
Title: Task scheduling for exploiting parallelism and hierarchy in VLSI CAD **algorithms**
Author: Belkhale, Krishna P.; Brouwer, Randall J.; Banerjee, Prithviraj
Corporate Source: Univ of Illinois, Urbana, IL, USA
Source: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems v 12 n 5 May 1993. p 557-567
Publication Year: 1993
CODEN: ITCSDI ISSN: 0278-0070
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical); A; (Applications)
Journal Announcement: 9311W1
Abstract: The computational requirements of computer-aided **design** problems are ever-increasing. One approach to handling this complexity is to take advantage of the hierarchical nature of circuit **design** and develop hierarchical **CAD** algorithms. Another approach to this problem involves the use of parallel processing and development of parallel **CAD** algorithms. In this paper, we discuss how these two approaches can be combined to speed up various **CAD** applications. Toward this goal, we formulate and solve two general problems in scheduling: 1) parallelizable independent task scheduling (PITS and 2) parallelizable dependent task scheduling (PDTS). Finally, we report on the use of the theory on two **VLSI CAD** applications. We present the application of our PITS scheduling theory to a parallel hierarchical circuit extractor, and the application of the PDTS scheduling theory to a parallel hierarchical global router. Both the implementations show speedups of about 6 on eight processors of a **shared memory** multiprocessor. (Author abstract) 35 Refs.
Descriptors: **VLSI** circuits; Computer aided **design** ; Algorithms; Hierarchical systems; Scheduling; Multiprocessing systems; Data storage equipment
Identifiers: **CAD** algorithms; **Hierarchical CAD** algorithms; **Shared memory** multiprocessors
Classification Codes:
714.2 (Semiconductor Devices & Integrated Circuits); 723.5 (Computer Applications); 722.1 (Data Storage, Equipment & Techniques)
714 (Electronic Components); 723 (Computer Software); 722 (Computer Hardware)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

14/5/10 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6964650 INSPEC Abstract Number: B2001-08-1265A-042, C2001-08-5210B-034
Title: Special session on low-power systems on chips (SOCs)
Author(s): Piguet, C.; Renaudin, M.; Omnes, T.J.-F.
Author Affiliation: CSEM, Neuchatel, Switzerland
Conference Title: Proceedings Design, Automation and Test in Europe. Conference and Exhibition 2001 p.488-94
Editor(s): Nebel, W.; Jerraya, A.
Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA
Publication Date: 2001 Country of Publication: USA xxxvi+829 pp.
ISBN: 0 7695 0993 2 Material Identity Number: XX-2001-00575
U.S. Copyright Clearance Center Code: 1530-1591/2001/$10.00
Conference Title: Proceedings Design, Automation and Test in Europe. Conference and Exhibition 2001
Conference Sponsor: EDAA; EDAC; IEEE-CS TTTC; IEEE-CS DATC; ECSI; RAS Russian Acad. Sci.; IPPM; ACM-SIGDA; IFIP 10.5; AEIA; ATI; CLRC; CNR; Estonian E Soc.; GI; GMM; HTE; ITG; KVIV; VDE
Conference Date: 13-16 March 2001 Conference Location: Munich, Germany
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: For innovative portable products, Systems on Chips (**SoCs**) containing several processors, memories and specialised modules are obviously required. Performances but also low-power are main issues in the **design** of such **SoCs** . Are these low-power **SoCs** only constructed with low-power processors, memories and logic blocks? If the latter are unavoidable, many other issues are quite important for low-power **SoCs** , such as the way to synchronise the communications between processors as well as test procedures, online testing, software **design** and development tools. This paper is a general framework for the **design** of low-power **SoCs** , starting from the system level to the **architecture** level, assuming that the **SoC** is mainly based on the re-use of low-power processors, memories and logic peripherals. **SoCs** with many processors, co-processors, memories and peripherals cannot be synchronised with a single master clock, due to larger and larger wire delays in deep submicron technologies. Several clocking schemes have been proposed, such as GALS (Globally Asynchronous Locally Synchronous) but also full asynchronous **architectures** . This paper will present the advantages and disadvantages of these **SoC** clocking strategies as well as the impacts on low power. For embedded **SoCs** containing several processors, one has to write several pieces of software for each processor starting typically from a high-level specification using the C/C++ language. In order to tackle this problem, we propose to first transform the original specification by means of a systematic script of platform-independent source code transformations. That is illustrated by applying global loop transformation techniques to identify asynchronous partitions exhibiting little communication and high locality of access characteristics. In a second stage, we explore multiple-instruction multiple-data (MIMD) mapping onto a given (partly) predefined platform using advanced space-time analysis techniques to maintain low data transfer rates while achieving high system throughput. At the **SoC** level, accurate cost feedback including high-level power estimation is required. From this essential information, energy trade-offs between application sub-modules can for example be used to refine the solution further. In the case of mapping onto programmable cores with a **shared memory hierarchy** , a final refinement consists in reorganising the data layout for efficient cache utilisation. (33 Refs)
Subfile: B C
Descriptors: application specific integrated circuits; asynchronous circuits; C language; delays; integrated circuit testing; logic testing; low-power electronics; **shared memory** systems; **VLSI**
Identifiers: low-power systems on chips; test procedures; online testing; software **design** ; development tools; logic peripherals; wire delays; deep submicron technologies; clocking schemes; GALS; full asynchronous **architectures** ; high-level specification; C++ language; C language; platform-independent source code transformations; global loop transformation techniques; multiple-instruction multiple-data mapping;

space-time analysis techniques; system throughput; high-level power estimation; energy trade-offs; programmable cores; **shared memory hierarchy** ; cache utilisation; locally synchronous

Class Codes: B1265A (Digital circuit design, modelling and testing); B2570A (Semiconductor integrated circuit design, layout, modelling and testing); C5210B (Computer-aided logic design); C5220P (Parallel architecture); C7410D (Electronic engineering computing)

14/5/11 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6467854 INSPEC Abstract Number: B2000-02-1265A-100, C2000-02-7410D-200
Title: An efficient bus architecture **for** system - on - chip design
Author(s): Cordan, B.
Author Affiliation: Palmchip Cor., Loveland, CO, USA
Conference Title: Proceedings of the IEEE 1999 Custom Integrated Circuits Conference (Cat. No.99CH36327) p.623-6
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA 668 pp.
ISBN: 0 7803 5443 5 Material Identity Number: XX-1999-01971
U.S. Copyright Clearance Center Code: 0 7803 5443 5/99/$10.00
Conference Title: Proceedings of the IEEE 1999 Custom Integrated Circuits Conference
Conference Sponsor: IEEE Solid States Circuits Soc
Conference Date: 16-19 May 1999 Conference Location: San Diego, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: This paper presents the issues confronted when integrating **system - on - chip (SOC) designs** and offers solution through a detailed description of the **CoreFrame** /sup TM/ **system - on - chip bus architecture** that has dramatically reduced system design and verification effort while enhancing the **reusability** and customizability of system-on-chip product developments. The **CoreFrame** on-chip **bus** architecture is defined along with examples to illustrate how a design friendly **bus** standard will effect the mix and match of **reusable cores** without sacrificing performance. (0 Refs)
Subfile: B C
Descriptors: application specific integrated circuits; circuit CAD; embedded systems; hardware-software codesign; integrated circuit design; **shared memory** systems; system **buses**
Identifiers: efficient **bus** architecture; **system - on - chip design ; CoreFrame ; reusability** ; customizability; system-on-chip product development; on-chip **bus** architecture; design friendly **bus** standard; mix and match; **reusable cores** ; intellectual property; PalmBus protocol; interface controller; **shared - memory** architecture
Class Codes: B1265A (Digital circuit design, modelling and testing); B2570A (Semiconductor integrated circuit design, layout, modelling and testing); B1130B (Computer-aided circuit analysis and design); C7410D (Electronic engineering computing); C5215 (Hardware-software codesign); C5610S (System buses)

Set	Items	Description
S1	13	AU=(BOYLAN, S? OR BOYLAN S?)
S2	31	AU=(COBURN, D? OR COBURN D?)
S3	45	AU=(CREEDON T? OR CREEDON, T?)
S4	7	AU=(DEPAOR D? OR DEPAOR, D? OR DE PAOR D? OR DE PAOR, D?)
S5	29	AU=(GAVIN V? OR GAVIN, V?)
S6	13	AU=(HYLAND K? OR HYLAND, K?)
S7	231	AU=(HUGHES S? OR HUGHES, S?)
S8	68	AU=(JENNINGS K? OR JENNINGS, K?)
S9	8	AU=(LARDNER M? OR LARDNER, M?)
S10	151	AU=(WALSH B? OR WALSH, B?)
S11	543	S1 OR S2 OR S3 OR S4 OR S5 OR S6 OR S7 OR S8 OR S8 OR S10
S12	29	S11 AND IC=(G06F-015? OR G06F-017?)
S13	29	IDPAT (sorted in duplicate/non-duplicate order)
S14	21	IDPAT (primary/non-duplicate records only)

File 347:JAPIO Nov 1976-2004/Mar(Updated 040708)
(c) 2004 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2004/Jul W02
(c) 2004 European Patent Office
File 349:PCT Fulltext 1979-2002/UB=20040708,UT=20040701
(c) 2004 WIPO/Univentio
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200445
(c) 2004 Thomson Derwent

14/5/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015313430 **Image available**
WPI Acc No: 2003-374365/200336
XRPX Acc No: N03-298567

Application specific integrated circuit design technique to design circuits composed of multiple functional blocks uses hardware description language to declare relevant signals and module instantiations

Patent Assignee: 3COM CORP (THRE-N); BOESEN B G (BOES-I); BOYLAN S T (BOYL-I); CREEDON T (CREE-I); GAVIN V G (GAVI-I); JENNINGS K (JENN-I); LARDNER M (LARD-I)

Inventor: BOESEN B G; **BOYLAN S ; CREEDON T ; GAVIN V ; JENNINGS K ;** LARDNER M; **BOYLAN S T ; GAVIN V G**

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
GB 2380818	A	20030416	GB 200124093	A	20011006	200336 B
US 20030101331	A1	20030529	US 20012980	A	20011206	200337
GB 2380818	B	20031119	GB 200124093	A	20011006	200376

Priority Applications (No Type Date): GB 200124093 A 20011006

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2380818	A		35	G06F-017/50	
US 20030101331	A1			G06F-015/00	
GB 2380818	B			G06F-017/50	

Abstract (Basic): GB 2380818 A

NOVELTY - Cores (1-12) are connected in an application specific integrated circuit with connections that constitute the hierarchical module interface (W), while each core represents a hardware description language. The numbers of levels in the hierarchy can be periodically different depending on the task.

USE - Designing application specific integrated circuit.

DESCRIPTION OF DRAWING(S) - The drawing shows plural cores

Cores (1-12)

Module interface (W)

pp; 35 DwgNo 1/12

Title Terms: APPLY; SPECIFIC; INTEGRATE; CIRCUIT; DESIGN; TECHNIQUE; DESIGN ; CIRCUIT; COMPOSE; MULTIPLE; FUNCTION; BLOCK; HARDWARE; DESCRIBE; LANGUAGE; RELEVANT; SIGNAL; MODULE

Derwent Class: T01

International Patent Class (Main): **G06F-015/00 ; G06F-017/50**

File Segment: EPI

14/5/8 (Item 8 from file: 350)

014856083 **Image available**
WPI Acc No: 2002-676789/200273
XRPX Acc No: N02-535011

Automatic generation of interconnected logic components using program tool relying on reusable elements to generate new and different architectures

Patent Assignee: 3COM CORP (THRE-N); BOYLAN S (BOYL-I); COBURN D (COBU-I); CREEDON T (CREE-I); DE PAOR D C (DPAO-I); GAVIN V G (GAVI-I); HUGHES S (HUGH-I); HYLAND K J (HYLA-I); JENNINGS K (JENN-I); LARDNER M (LARD-I); WALSH B (WALS-I)

Inventor: **BOYLAN S ; COBURN D ; CREEDON T ; DE PAOR D ; GAVIN V ; HUGHES S M ; HYLAND K J ;** JENNING K; LARDNER M; **WALSH B ; DE PAOR D C ; GAVIN V G ; HUGHES S ; JENNINGS K**

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
GB 2372851	A	20020904	GB 200118840	A	20010802	200273 B
US 20030018738	A1	20030123	US 2001919806	A	20010802	200310
GB 2372851	B	20030319	GB 200118840	A	20010802	200321

Priority Applications (No Type Date): GB 20014945 A 20010228

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2372851	A		68	G06F-017/50	
US 20030018738	A1			G06F-017/50	
GB 2372851	B			G06F-017/50	

Abstract (Basic): GB 2372851 A

NOVELTY - The multiple-bus paths for a system-on-chip include elements that can be obtained from a library and elements which will have to be generated as part of the interconnection logic and the figure shows upward paths, from cores to target memory and downward paths, from memory to cores of data transactions on the memory bus. The paths pass through arbitrators to arbitrate access to memory by a data aggregation technique.

USE - Generation of large scale integrated circuits by layout of system-on-chip.

DESCRIPTION OF DRAWING(S) - The drawing shows bus paths.

pp; 68 DwgNo 11/13

Title Terms: AUTOMATIC; GENERATE; INTERCONNECT; LOGIC; COMPONENT; PROGRAM; TOOL; RELY; REUSE; ELEMENT; GENERATE; NEW

Derwent Class: T01; U11

International Patent Class (Main): **G06F-017/50**

International Patent Class (Additional): **G06F-015/167**

File Segment: EPI

14/5/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014622793 **Image available**
WPI Acc No: 2002-443497/200247
XRPX Acc No: N02-349430

Multi-port assembly in networks such as ethernet, has cache controller which allows address look-up when address pair in packet is not held in cache and updates cache with entries of high traffic flow

Patent Assignee: 3COM CORP (THRE-N); JENNINGS K (JENN-I); NOLAN D (NOLA-I); NOLAN J (NOLA-I); O'CALLAGHAN S (OCAL-I); O'KEEFFE P (OKEE-I)
Inventor: **JENNINGS K** ; NOLAN D; NOLAN J; O'CALLAGHAN S; O'KEEFE P; O'KEEFFE P
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020046291	A1	20020418	US 2000725476	A	20001130	200247	B
GB 2368228	A	20020424	GB 200025507	A	20001018	200247	
GB 2368228	B	20030723	GB 200025507	A	20001018	200356	

Priority Applications (No Type Date): GB 200025507 A 20001018
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020046291	A1		11	G06F-015/16	
GB 2368228	A			H04Q-011/04	
GB 2368228	B			H04Q-011/04	

Abstract (Basic): US 20020046291 A1

NOVELTY - A cache controller determines whether the address pair in a packet is held in the cache in response to a look-up request. The look-up engine performs address look-up, when the address pair is not held in cache. The cache memory is updated using entries corresponding to high measures of traffic flow.

USE - Used in networks such as ethernet, virtual local area network, etc, to determine the destination of the packet.

ADVANTAGE - The cache is continually updated with respect to the traffic flow.

DESCRIPTION OF DRAWING(S) - The figure shows the explanatory diagram of packet search process.

pp; 11 DwgNo 4/7

Title Terms: MULTI; PORT; ASSEMBLE; NETWORK; CACHE; CONTROL; ALLOW; ADDRESS ; UP; ADDRESS; PAIR; PACKET; HELD; CACHE; UPDATE; CACHE; ENTER; HIGH; TRAFFIC; FLOW
Derwent Class: T01; W01
International Patent Class (Main): **G06F-015/16** ; H04Q-011/04
International Patent Class (Additional): H04L-012/56; H04L-029/06; H04Q-003/00
File Segment: EPI